

| Course Number | COE328 |
| --- | --- |
| Course Title | Digital Systems - F2022 |
| Semester/Year | Fall 2022 |
| Instructor | Shazzat Hossain |
| TA Name | Sajjad |

| Lab/Tutorial Report No. | Lab 4 |
| --- | --- |

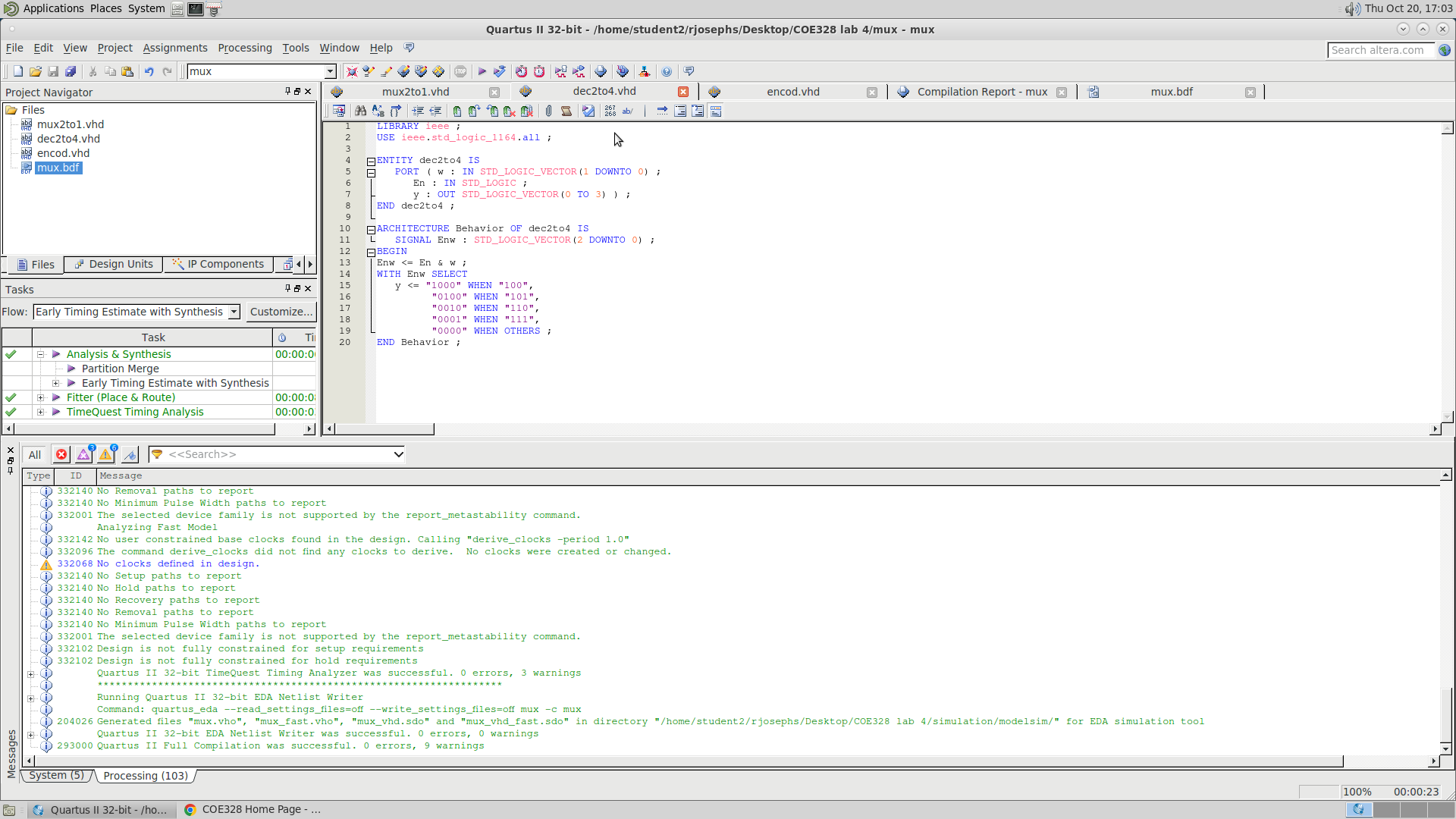
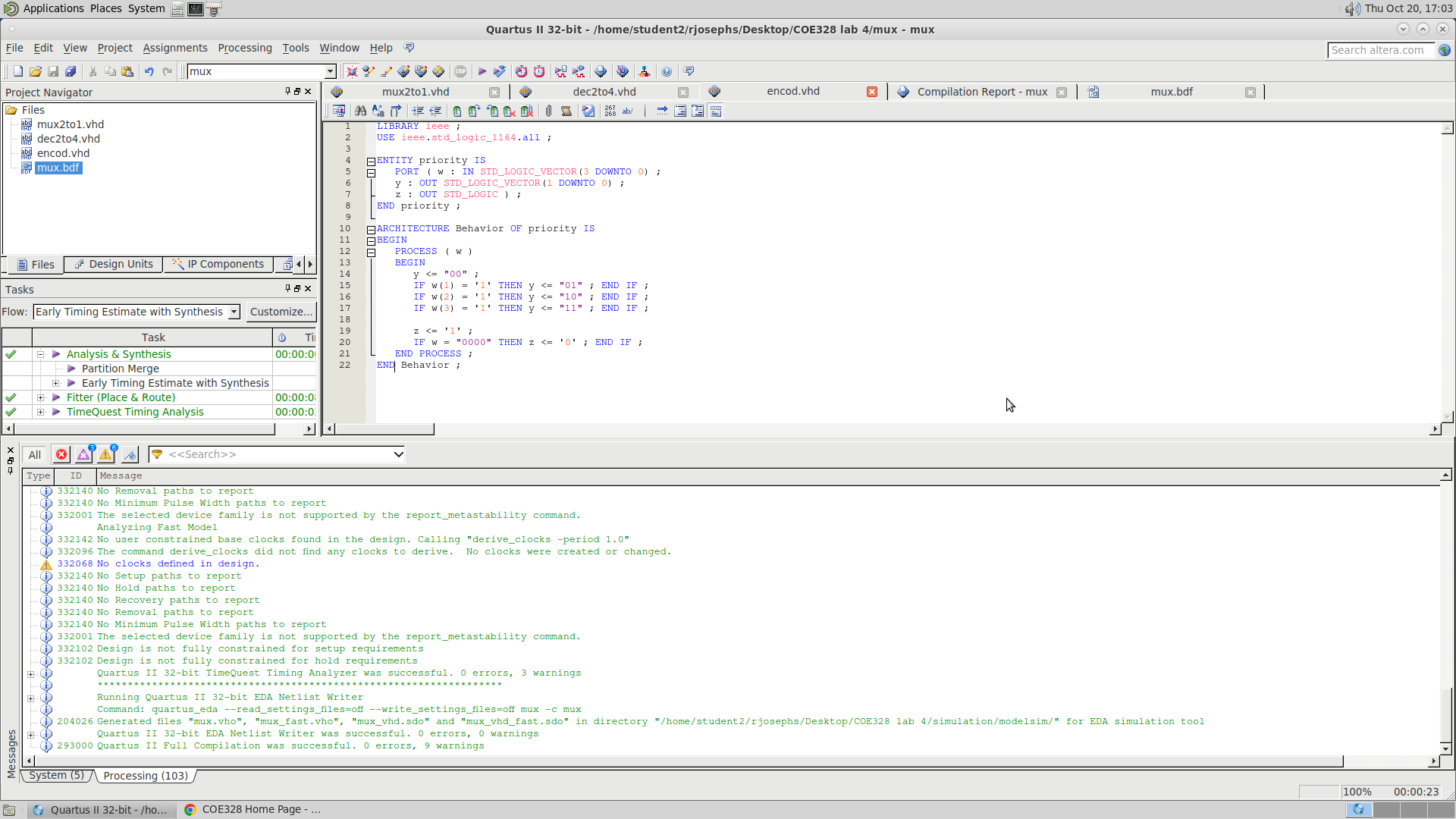
| Report Title | **VHDL for Combinational Circuits and Storage Elements** |
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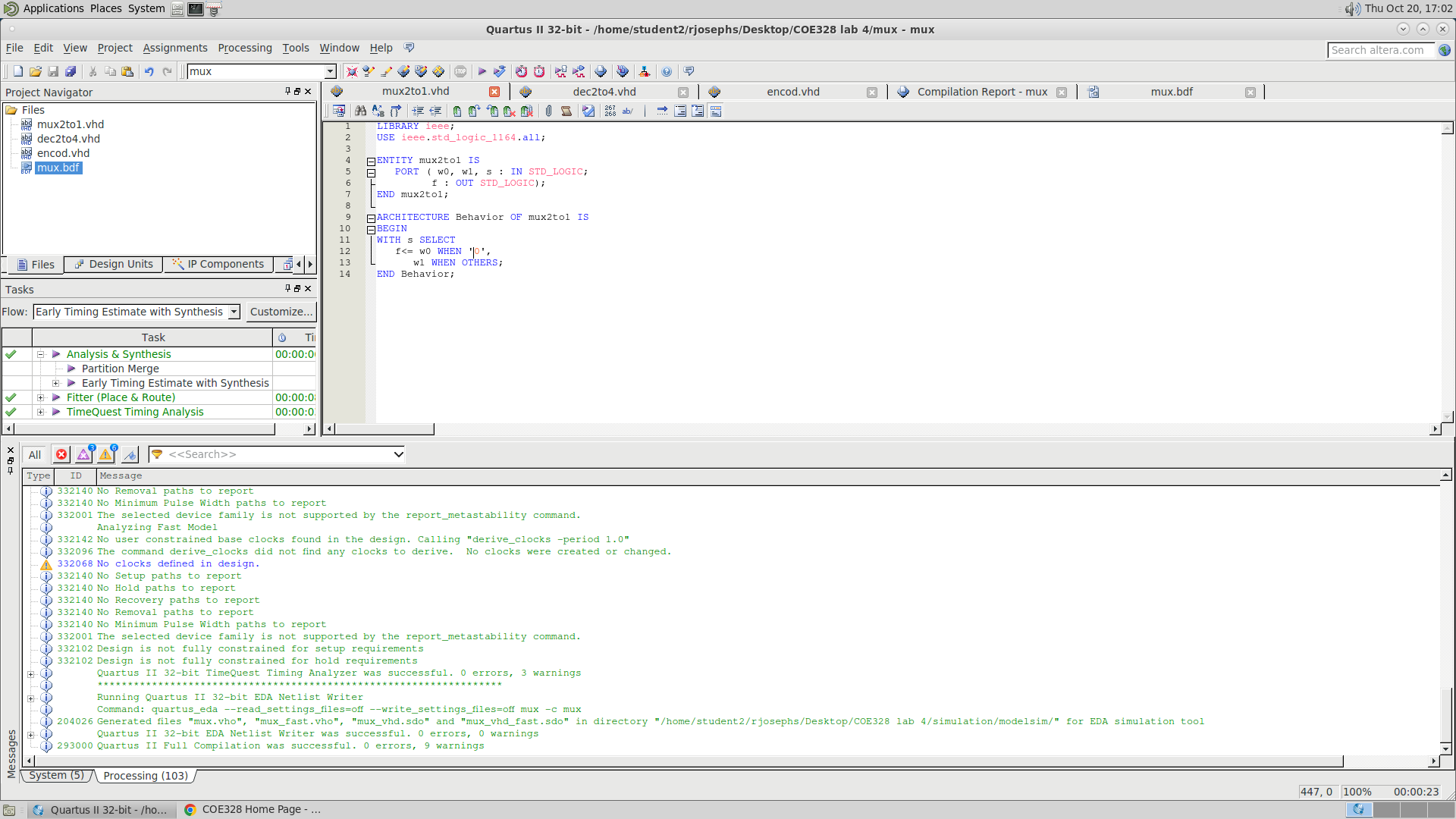
| Section No. | 11 |
| --- | --- |
| Group No. | N/A |
| Submission Date | December 2, 2022 |
| Due Date | December 3, 2022 |

| Student Name | Student ID | Signature\* |
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| Hamza Malik | 501112545 | Hamza Malik |

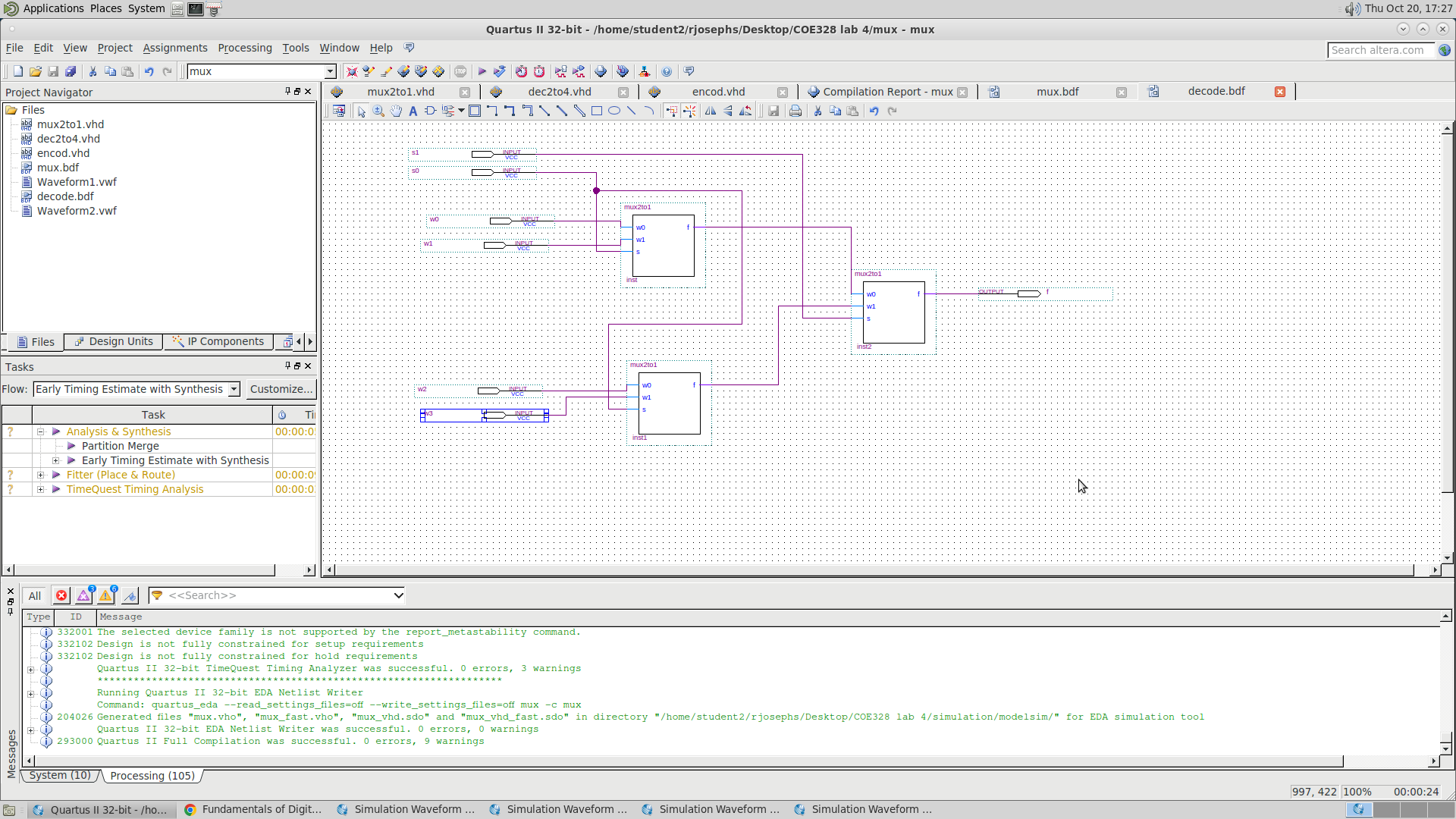
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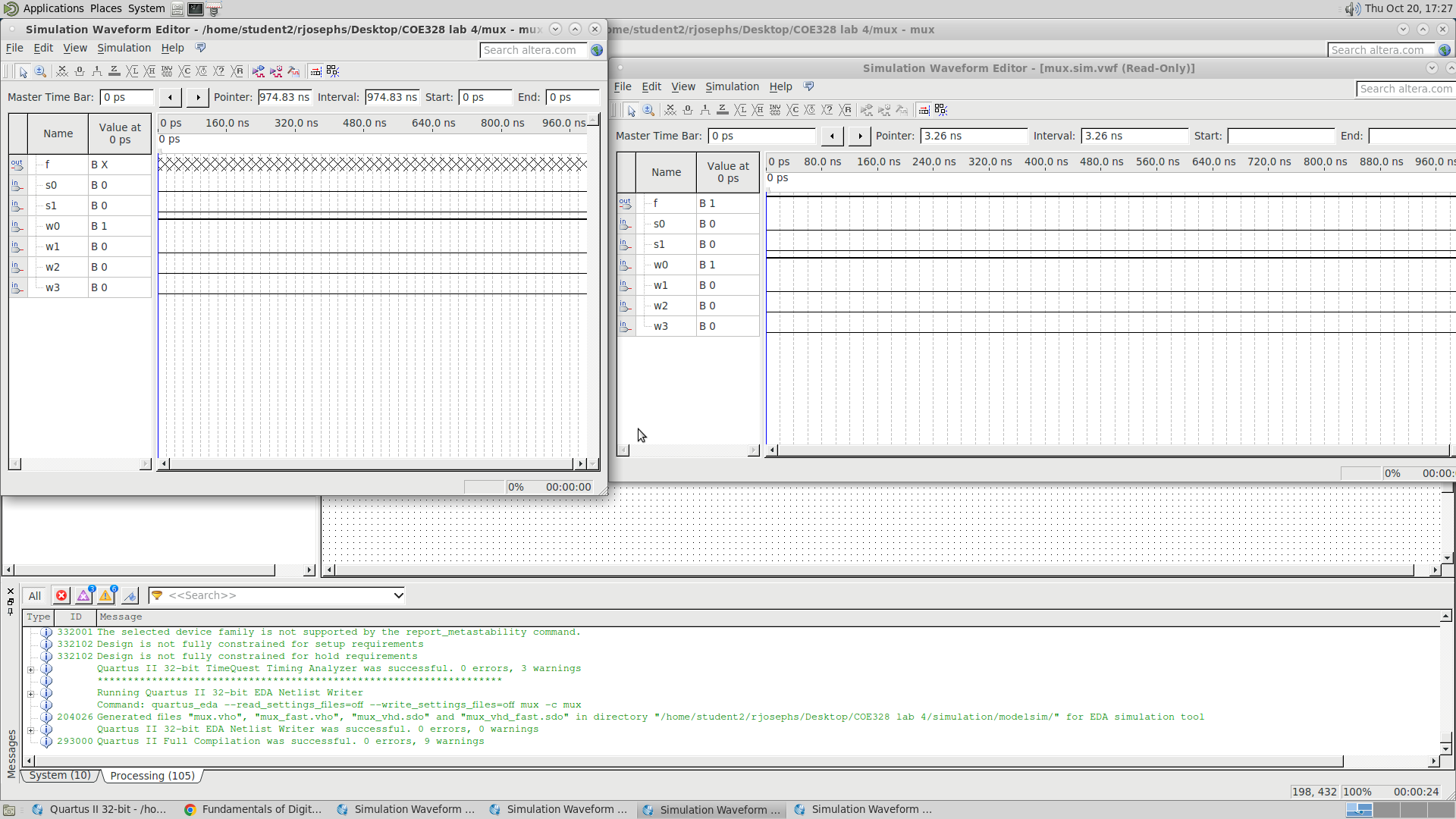


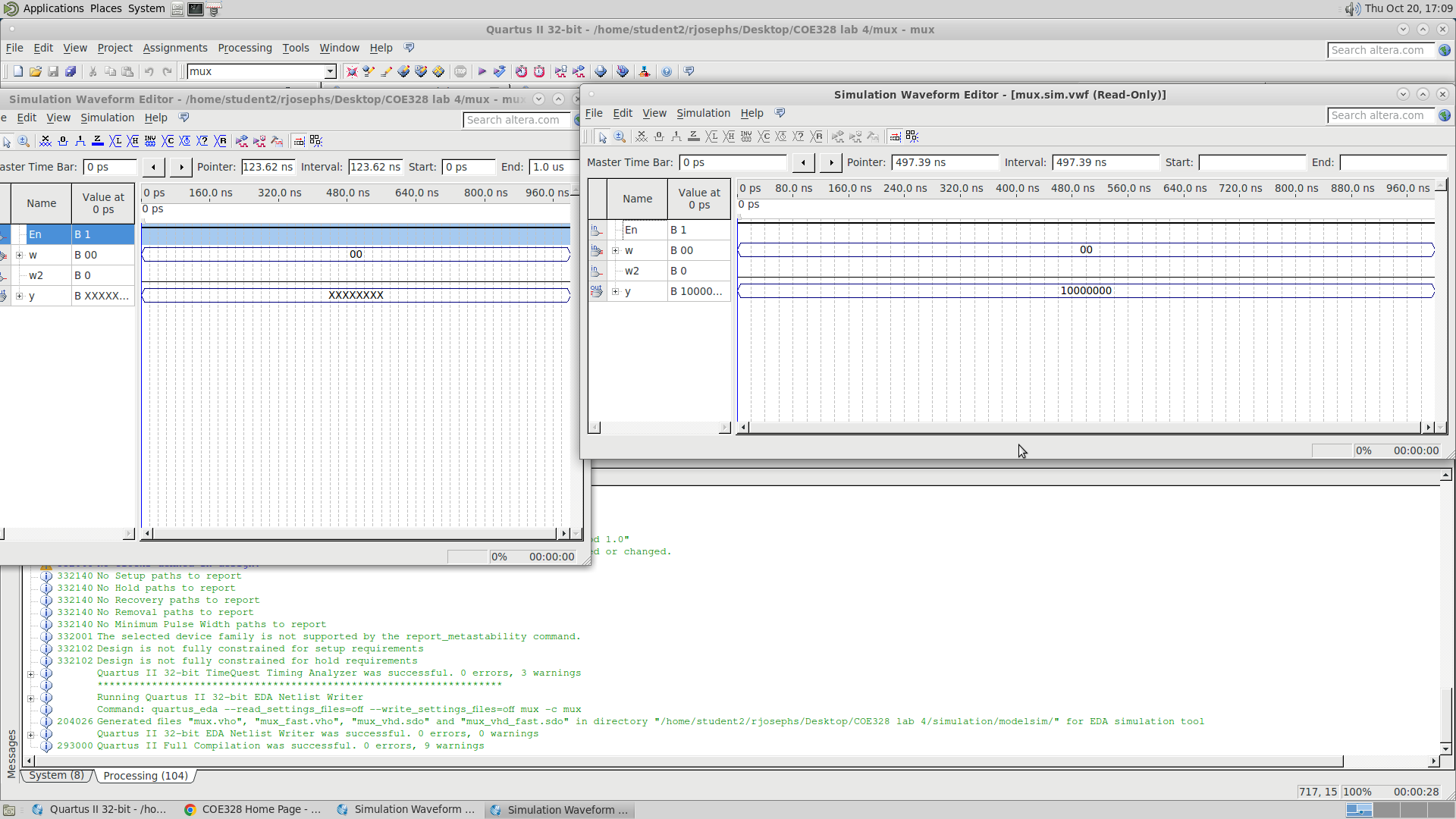


This is the VHDL Skeleton code for lab4 part 1 coe328 created during our lab 4 week 1 with the custom function.

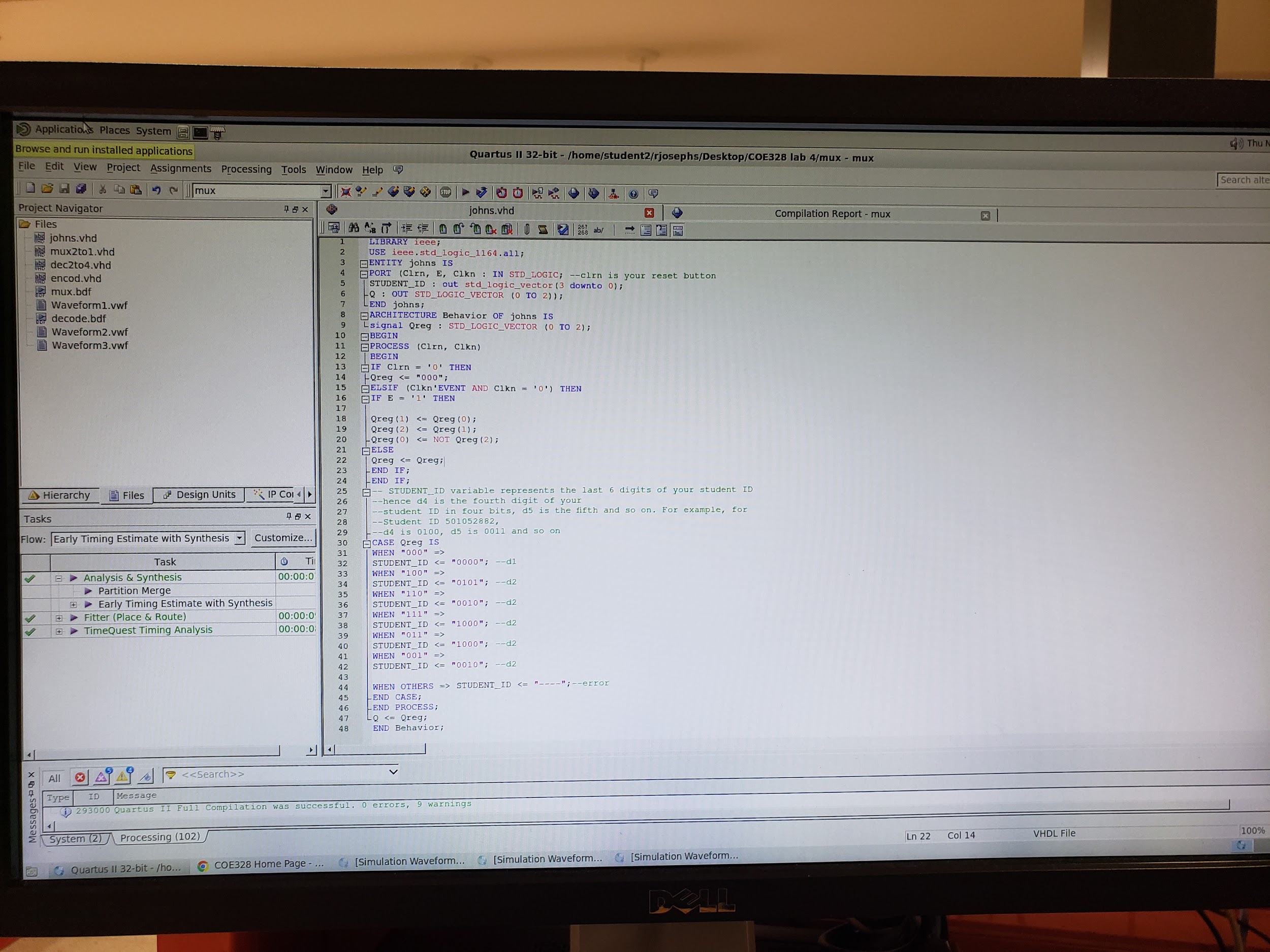


This is our block diagram schematics symbol made using the vdhl code for lab4 part 1

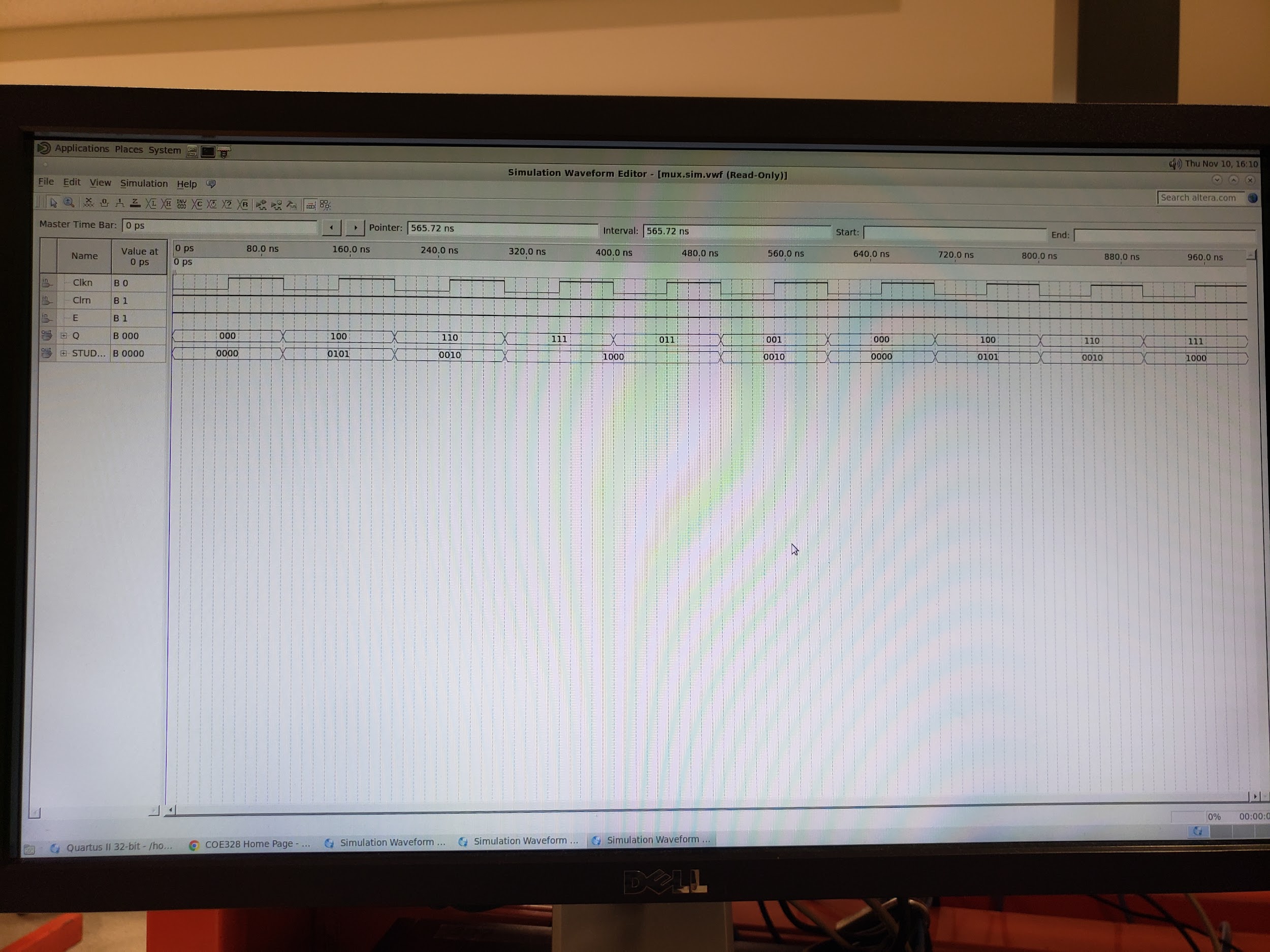




This is a picture of our waveform diagram created with the VHDL code for lab4 part 1.



This is the VHDL Skeleton code for lab4 part 2 coe328 created during our lab 4 week 2 with the custom function.



This is a picture of our waveform diagram created with the VHDL code for lab4 part 2.

**Conclusion:**

To wrap up our lab 4, we constructed combinational circuits and circuits with basic storage elements. The lab was broken down into 2 weeks, for the first week we used subdirectories from our prelab to implement our vdhl code with our student numbers then implemented 4:1 multiplexer using two 2:1 multiplexer and got our overall waveform output. For the second week we implemented the Johnson counter with our student number, got the vdhl code and the overall wave form output.